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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/758,675	01/11/2001	Klaus Gloeckler	10191/1639	9544

26646 7590 07/09/2003

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EXAMINER
TORRES, JOSEPH D

ART UNIT	PAPER NUMBER
2133	6

DATE MAILED: 07/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/758,675	GLOECKLER ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☒ Claim(s) *10-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 January 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings are objected to because the steps in Figure 2 lack meaningful labels (Note: MPEP § 608.02 states, "Symbols with unclear meanings should be labeled for clarification"). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: The Examiner asserts that the Applicant's use of the word "level" (e.g., lines 18-19, page 4 of the Applicant's specification cites, "The levels present can then be measured") is arbitrary, vague and indefinite. The Authoritative Dictionary of IEEE Standards Terms defines level as a magnitude, especially when considered in relation to an arbitrary reference value. Without saying what the level is (i.e., Is it a voltage, current or some other quantity?) it would be impossible for one of ordinary skill in the art at the time the invention was made to make or use of any of the teachings associated with such language.

Appropriate correction is required.

Claim Objections

3. Claims 10-12 are objected to because of the following informalities: Claim 10 cites, "a test routine **capable of** being executed on the at least one microprocessor" [Emphasis Added]. The Examiner asserts that capable implies that the microprocessor only has to be capable of executing a test routine which any microprocessor is capable of, but does not require the that the test routine be executed, hence "being executed on the at least one microprocessor" does not limit the scope of claim 10.

4. Claim 12 cites, "one of levels present **can be** measured and defined values **can be** applied from outside the microcontroller" [Emphasis Added]. The Examiner asserts that **can be** implies that the one of levels present only has to be capable of being measured and defined, and applied from outside the microcontroller, but does not require the that the one of levels present be measured and defined, and applied from outside the microcontroller, hence "measured and defined values, and applied from outside the microcontroller" does not limit the scope of claim 12, since measuring and defining values, and applying from outside the microcontroller does not necessarily have to happen.

Claims 11 and 12 depend from claim 10 hence inherit the deficiencies of claim 10.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the

art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 5 and 12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 5 cites "measuring **levels**" and claim 12 cites, "wherein one of **levels** present can be measured" [Emphasis Added].

The Examiner asserts that the Applicant's use of the word "level" is arbitrary, vague and indefinite. The Authoritative Dictionary of IEEE Standards Terms defines level as a magnitude, especially when considered in relation to an arbitrary reference value. Without saying what the level is (i.e., Is it a voltage, current or some other quantity?) it would be impossible for one of ordinary skill in the art at the time the invention was made to make or use any of the teachings associated with such language.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. Claim 1 cites, a "method for activating a microprocessor arranged as a part of a microcontroller, within a framework of a boundary scan test procedure **according to** IEEE standard 1149, **in accordance with** a JTAG interface" [Emphasis Added]. The

omitted structural cooperative relationships are: the relationship between a "method for activating a microprocessor arranged as a part of a microcontroller, within a framework of a boundary scan test procedure" and "IEEE standard 1149" and "a JTAG interface" since "in accordance with" and "according to" do not set forth the relationship required for providing a "method for activating a microprocessor arranged as a part of a microcontroller, within a framework of a boundary scan test procedure" given "a test routine that is executable on the microprocessor".

Claims 2-9 depend from claim 1 hence inherit the deficiencies of claim 1.

Claim 10 cites similar language as in claim 1.

Claims 11 and 12 depend from claim 10 hence inherit the deficiencies of claim 10.

6. Claims 1-9 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

Claim 1 cites, "the step of activating the JTAG interface of the microprocessor **in accordance with** a test routine that is executable on the microprocessor" [Emphasis Added]. The omitted structural cooperative relationships are: the relationship between "activating the JTAG interface of the microprocessor" and "a test routine that is executable on the microprocessor" since "in accordance with" does not set forth the relationship required for "activating the JTAG interface of the microprocessor" given "a test routine that is executable on the microprocessor".

Claim 2 cites, "activating the pins of the JTAG interface **in accordance with** the test routine via the I/O ports". [Emphasis Added]. The omitted structural cooperative relationships are: the relationship between "activating the pins of the JTAG interface" and "the test routine via the I/O ports".

Claim 3 cites, "a reading operation with respect to the pins of the JTAG interface **in accordance** with a stipulated test sequence in the test routine". [Emphasis Added]. The omitted structural cooperative relationships are: the relationship between "a reading operation with respect to the pins of the JTAG interface" and "a stipulated test sequence in the test routine".

Claim 3 cites, "performing at least one of a setting operation and a reading operation **with respect to** the pins of the JTAG interface". [Emphasis Added]. The omitted structural cooperative relationships are: the relationship between "performing at least one of a setting operation and a reading operation" and "the pins of the JTAG interface" since "**with respect to**" does not set forth the relationship required for "performing at least one of a setting operation and a reading operation" given "the pins of the JTAG interface".

Claim 5 cites, "switching the I/O ports of the microprocessor in accordance with the test routine". [Emphasis Added]. The omitted structural cooperative relationships are: the relationship between "switching the I/O ports of the microprocessor" and "the test routine".

Claim 6 cites, "switching the I/O ports of the microprocessor in accordance with the test routine". [Emphasis Added]. The omitted structural cooperative relationships are: the

relationship between "switching the I/O ports of the microprocessor" and "the test routine".

Claim 6 cites, "applying defined values to an interface of the microcontroller in accordance with the stipulated test sequence". [Emphasis Added]. The omitted structural cooperative relationships are: the relationship between "applying defined values to an interface of the microcontroller" and "the stipulated test sequence".

7. Claims 5 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 cites "measuring **levels**" and claim 12 cites, "wherein one of **levels** present can be measured" [Emphasis Added].

The Examiner asserts that the Applicant's use of the word "level" is arbitrary, vague and indefinite since by the dictionary definition of the word a level is any magnitude (The Authoritative Dictionary of IEEE Standards Terms defines level as a magnitude, especially when considered in relation to an relation to an arbitrary reference value).

8. Claims 5 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: the type of level that is claimed by the claim language in claims 5 and 12.

The Examiner asserts that claims 1-12 are replete with 35 U.S.C. 112 problems and the claims need to be reviewed and revised to remove all of the 35 U.S.C. 112 problems some of which are listed, above.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-8 and 10-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Zuraski, Jr., Gerald D. et al. (US 6560740 B1, hereafter referred to as Zuraski).

35 U.S.C. 102 rejection of claims 1 and 10.

Zuraski teaches a method for activating a microprocessor arranged as a part of a microcontroller (Microprocessor 10 in Figure 1 of Zuraski is a microcontroller and CPU Core 14 is a microprocessor; Note: a microcontroller is defined as an integrated circuit comprising a microprocessor and one or more peripherals, hence Microprocessor 10 in Figure 1 of Zuraski is a microcontroller with microprocessor, CPU Core 14, and peripherals, Embedded Memory Units 16a-16b), within a framework of a boundary scan test procedure according to IEEE standard 1149, in accordance with a JTAG interface

(col.5, lines 56-65 in Zuraski teaches that Microprocessor 10 is configured to implement Joint Test Action Group or JTAG boundary scan testing of logic 12 according to IEEE Standard 1149.1-1990 controlled by a test control unit 26 of the boundary scan test system), comprising the step of activating the JTAG interface of the microprocessor in accordance with a test routine that is executable on the microprocessor (col. 6, lines 9-16, Zuraski teach that prior to initiation of the programmable BIST routine, the microprocessor, CPU core 14, may store the programmable test data within addressable registers of special register block 15 **in response to software instructions**; Note: software instructions are executable code).

35 U.S.C. 102 rejection of claims 2 and 11.

Zuraski teaches a I/O ports of the microprocessor are connected to pins of the JTAG interface (see I/O terminals 24 in Figure 1 of Zuraski), the method further comprising the step of: activating the pins of the JTAG interface in accordance with the test routine via the I/O ports (col. 6, lines 1-6, Zuraski teaches a hardwired BIST routine performed automatically following assertion of a RESET signal received by the microprocessor via an I/O terminal 24).

35 U.S.C. 102 rejection of claims 3 and 4.

See col. 8, lines 17-19, Zuraski; Note: Zuraski teaches that during BIST testing, data is written to and/or read from the rows of memory locations within embedded memory

units 16a-b. In addition a reset operation is an embodiment of a set operation (see rejection to claims 2 and 11, above).

35 U.S.C. 102 rejection of claims 5 and 6.

See col. 7, lines 1-7, Zuraski. Note: Zuraski teaches that during normal operation of microprocessor 10, signals upon I/O terminals 24 flow to and from logic 12 unimpeded and during boundary scan testing, test control unit 26 configures boundary scan cells 22 to form a serial "scan chain" surrounding logic 12. Input values, produced by external circuitry, are shifted through the scan chain, then applied to logic 12. In addition, output values produced by logic 12 are captured by a portion of boundary scan cells 22, shifted out through the scan chain, and compared to expected values.

35 U.S.C. 102 rejection of claim 7.

See Special Register Block 15 in Figure 1 of Zuraski for storing test data (col. 7, lines 61-67, Zuraski).

35 U.S.C. 102 rejection of claims 8 and 12.

See col. 7, lines 1-7, Zuraski. Note: Zuraski teaches that output values produced by logic 12 are captured by a portion of boundary scan cells 22, shifted out through the scan chain, and compared to expected values.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zuraski, Jr., Gerald D. et al. (US 6560740 B1, hereafter referred to as Zuraski) in view of Margolis, Donald L. et al. (US 5357432 A, hereafter referred to as Margolis).

35 U.S.C. 103(a) rejection of claim 9.

Zuraski, substantially teaches the claimed invention described in claims 1-8 (as rejected above).

However Zuraski, does not explicitly teach the specific use of the microcontroller taught in the Zuraski patent **for a motor vehicle**.

Margolis, in an analogous art, teaches a microcontroller for use in a sensing system for a motor vehicle (col. 4, lines 60-68, Margolis). The Examiner asserts that it would be

obvious to use the microcontroller taught in the Zuraski patent since that is what a microcontroller is designed for. One of ordinary skill in the art at the time the invention was made would have been highly motivated to use the microcontroller taught in the Zuraski patent in a motor vehicle because the microcontroller taught in the Zuraski patent has the added feature of Built-In Self-Test (BIST) logic which provides the ability to test for circuit integrity and to repair circuit failures to maintain circuit integrity (see Abstract, Zuraski).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Zuraski with the teachings of Margolis by including use of the microcontroller taught in the Zuraski patent in a motor vehicle. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of the microcontroller taught in the Zuraski patent in a motor vehicle would provide the opportunity to test for circuit integrity and to repair circuit failures to maintain circuit integrity (see Abstract, Zuraski).

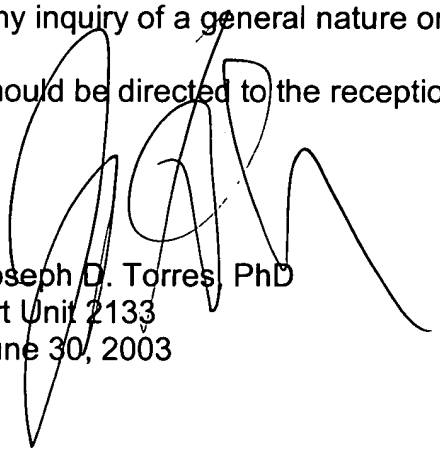
Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Carbonaro, Joseph et al. (US 5003286 A) teaches a microcontroller is defined as an integrated circuit comprising a microprocessor and one or more peripherals.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-746-7240.



Joseph D. Torres, PhD
Art Unit 2133
June 30, 2003